IN THE SPECIFICATION

1. Replace the paragraph beginning on page 5 at line 12 with the following paragraph:

Spread spectrum clock system 11 includes a spread spectrum clock source 14 and a power supply 15. Clock source 14 provides the clock signal for circuit 10, while power supply 15 provides the supply voltage signal V_{dd} for the circuit. As used in this disclosure and the accompanying claims, "supply voltage signal" refers to the voltage signal supplied to and distributed throughout circuit 10 to provide the electrical energy required to operate the various components of the circuit. Also, "clock signal" refers to the signal comprising a suitable clock waveform which is supplied to circuit 10 and distributed throughout the circuit to clock or coordinate the operation of various components in the circuit.

2. Replace the paragraph beginning on page 6 at line 3 with the following paragraph:

Although the power supply 15 is shown as an operational amplifier in Figure 1, it will be appreciated that the invention may be implemented using any suitable power supply arrangement. A suitable power supply for purposes of this invention and the accompanying claims comprises any power supply in which the output supply voltage may be modulated. Even in the operational amplifier arrangement shown in Figure 1, filters and other signal conditioning arrangements may be included with the power supply. These additional components which may be included in the power supply 15 are omitted from the figures so as not to obscure the invention in unnecessary detail.

3. Replace the paragraph beginning on page 6 at line 12 with the following paragraph:

Spread spectrum clock source 14 shown in Figure 1 comprises a phase lock loop (PLL) arrangement including a phase detector 21, loop filter 22, and voltage controlled oscillator (VCO) 23. A divider may be included in the feedback path of the PLL circuit, but is omitted from Figure 1 in order to ~~simply~~ simplify the drawing. A summing method 27 is also included in the PLL clock source in this preferred form of the invention. The PLL clock source receives an oscillator or base frequency input B and a modulation input at 28. Base frequency B is applied as one input to phase detector 21 and provides a reference to which the clock source output signal at node 26 may be locked. The signal at modulation input 28 is summed as indicated by summing method 27 to produce a modulated signal at an input 25 to VCO 23. This modulated signal modulates the frequency of the clock signal output 26 so that the clock frequency varies within a certain range about a center or nominal frequency. It should be noted that if modulation input 28 to summing method 27 is zero, then the signal at VCO input 25 is identical to that of the output 29 from loop filter 22, as would be the case for a conventional PLL clock source.